Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-20 (Canceled)

Claims 21-40 (Canceled)

Claim 41 (new) A System-on-Chip (SOC) semiconductor device designed with an architecture with a latency tolerant signal protocol, comprising:

one or more processor cores, one or more peripherals, one or more DMA-type peripherals, and a memory subsystem;

a first internal bus coupled to said processor core(s) and to said peripheral(s), said first internal bus uses an architecture with a latency tolerant signal protocol that carries signals from signal initiators to signal targets;

wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stage(s) are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration; and

a second internal bus coupled to said processor core(s), said memory subsystem, and said DMA-type peripheral(s), said second internal bus uses said architecture with said latency tolerant signal protocol that carries signals from signal initiators to signal targets;

wherein said architecture with said latency tolerant signal protocol of said second internal bus provides for said arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stage(s) are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration.

Claim 42 (new) A method to manufacture a System-on-Chip (SOC) semiconductor device designed with an architecture with a latency tolerant signal protocol, comprising:

providing one or more processor cores, one or more peripherals, one or more DMA-type peripherals, and a memory subsystem;

providing a first internal bus coupled to said processor core(s) and to said peripheral(s), said first internal bus uses an architecture with a latency tolerant signal protocol that carries signals from signal initiators to signal targets;

wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stage(s) are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration; and

providing a second internal bus coupled to said processor core(s), said memory subsystem, and said DMA-type peripheral(s), said second internal bus uses said architecture with said latency tolerant signal protocol that carries signals from signal initiators to signal targets;

wherein said architecture with said latency tolerant signal protocol of said second

internal bus provides for said arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stage(s) are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration.

Claim 43 (new) A method to use a System-on-Chip (SOC) semiconductor device designed with an architecture with a latency tolerant signal protocol, comprising:

providing one or more processor cores, one or more peripherals, one or more DMA-type peripherals, and a memory subsystem;

carrying signals from signal initiators to signal targets with a first internal bus coupled to said processor core(s) and to said peripheral(s), said first internal bus uses an architecture with a latency tolerant signal protocol;

wherein said architecture with said latency tolerant signal protocol of said first internal bus provides for an arbitrary number of pipeline stages between any signal initiator and any signal target wherein said arbitrary number of pipeline stage(s) are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration;

carrying signals from signal initiators to signal targets with a second internal bus coupled to said processor core(s), said memory subsystem, and said DMA-type peripheral(s), said second internal bus uses said architecture with said latency tolerant signal protocol;

wherein said architecture with said latency tolerant signal protocol of said second internal bus provides for said arbitrary number of pipeline stages between any signal

initiator and any signal target wherein said arbitrary number of pipeline stage(s) are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration.

Claim 44 (new) A dependent claim according to claims 41, 42, or 43 wherein said signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking.

Claim 45 (new) A dependent claim according to claims 41, 42, or 43 wherein said arbitrary number of pipeline stages further comprise one or more of the following: flip-flop(s), multiplexing router(s), or decoding router(s).

Claim 46 (new) A dependent claim according to claims 41, 42, or 43 wherein said first internal bus and said second internal bus have overlapping topologies, each topology further comprising one or more of the following topologies: matrix fabric (or woven) topology, point-to-point topology, bridged topology, or bussed topology.